System on a Chip

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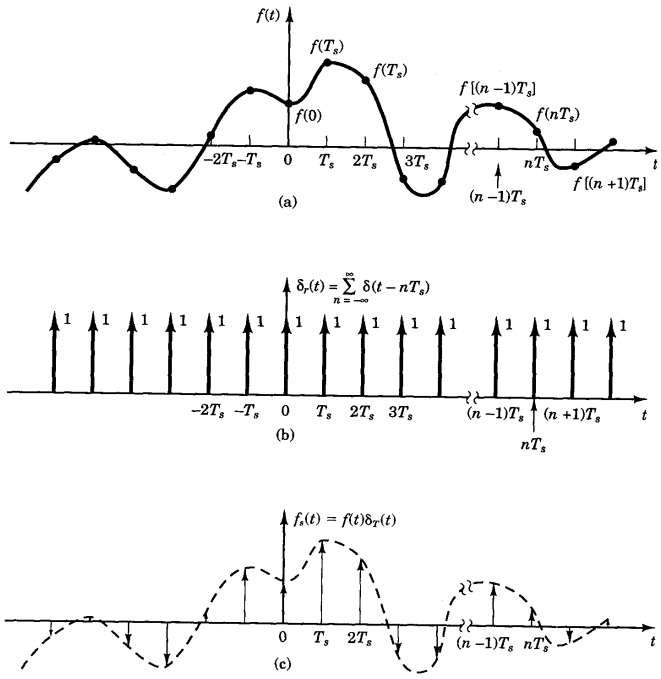
Lecture 5:
Data Conversion

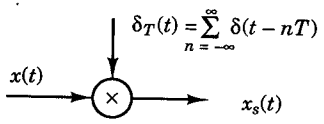
- ADC
  - Background/Theory
  - Examples

Background

- Physical systems are typically analogue
- To apply digital signal processing, the analogue signal has to be converted to a digital signal
- Analogue signals are analogue in amplitude and time
- Digital signals are discrete in amplitude and time
- A/D conversion:
- Step 1: sample the analogue signal (to make the signal time discrete)
- Step 2: Digitising (to make the signal amplitude discrete)
- Many A/D conversion methods exist; trade-off between bandwidth, accuracy, circuit complexity, cost, power consumption, etc.

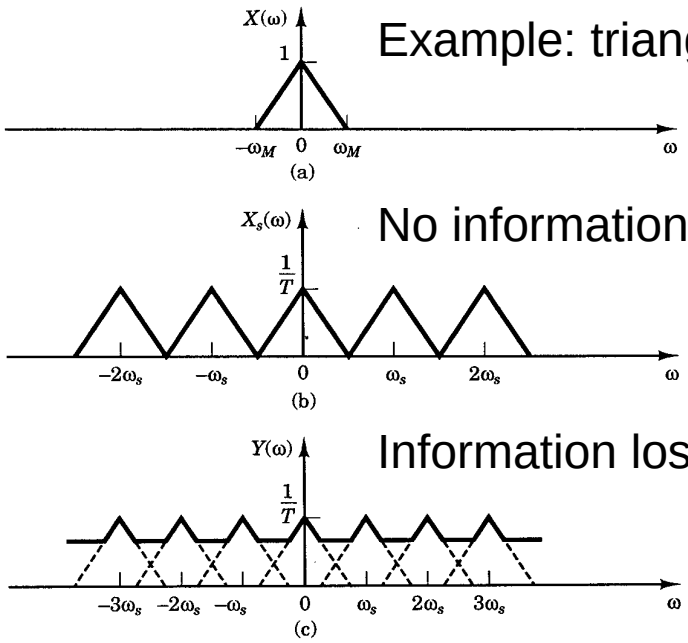
Ideal Sampling





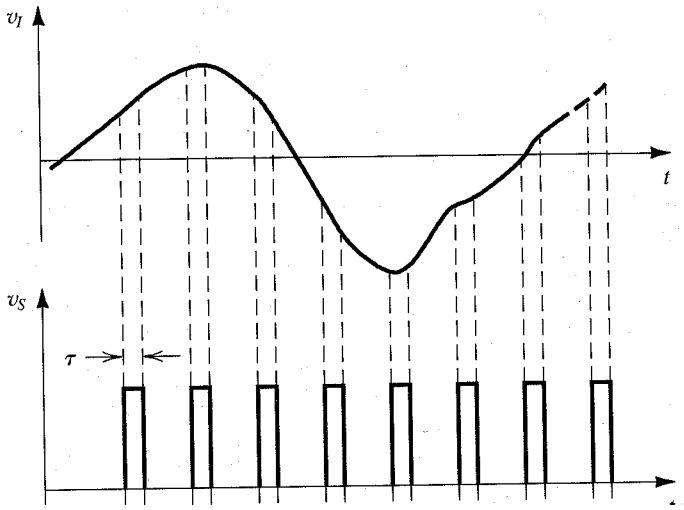
- Sampling: generation of an ordered number sequence by taking values of x(t) at specific instants of time
- Mathematical representation: analogue signal is multiplied by an impulse comb

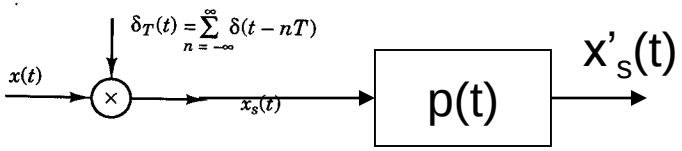
Ideal Sampl. – Frequency Domain



- Assume that x(t) is bandlimited; i.e. $X(\omega) = 0$ for $\omega > \omega_m$
- If the highest frequency in X(w) is smaller than half the sampling frequency (the Nyquist frequency), the spectrum of $x_s(t)$ is identical to that of x(t), but repeated with a period of ω_s. Consequently, no information is lost (Shannon's Theorem)
- Otherwise the spectra overlap and information is lost

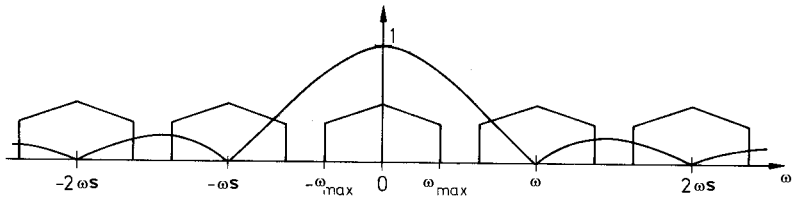
Real Sampl. – Frequency Domain





- In practice, an impulse comb is not possible, it is approximated by a square with width τ
- p(t) is a string of rectangles

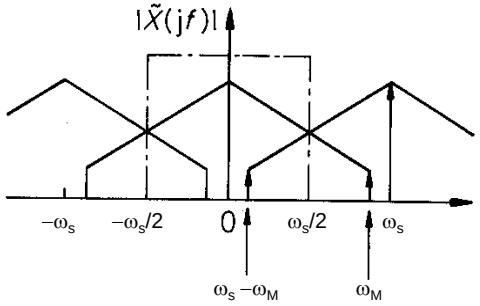
Real Sampl. – Frequency Domain

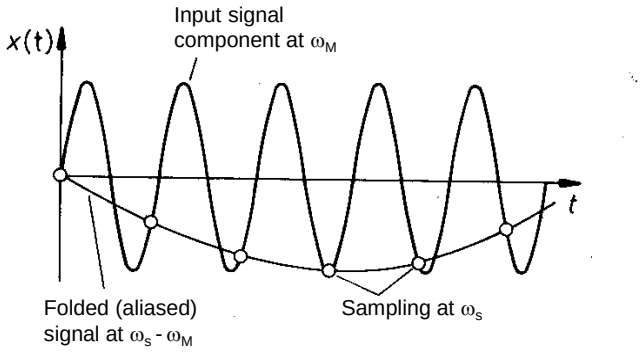


In this case the width τ is equal to $1/f_s$, which is the case for a sample and hold that usually precedes an A/D converter.

- Using squares instead of an impulse comb has the effect that the original spectrum magnitude is multiplied by $\sin(\pi f/f_s)/(\pi f/f_s)$
- This results in an amplitude reduction of the original spectrum. For Nyquist sampling the reduction is -3.92dB if a sample and hold is used
- Oversampling can be used to alleviate the problem. If the signal is oversampled by 4 times the Nyquist rate ($\omega_s = 8\omega_M$), the reduction drops to -0.22dB

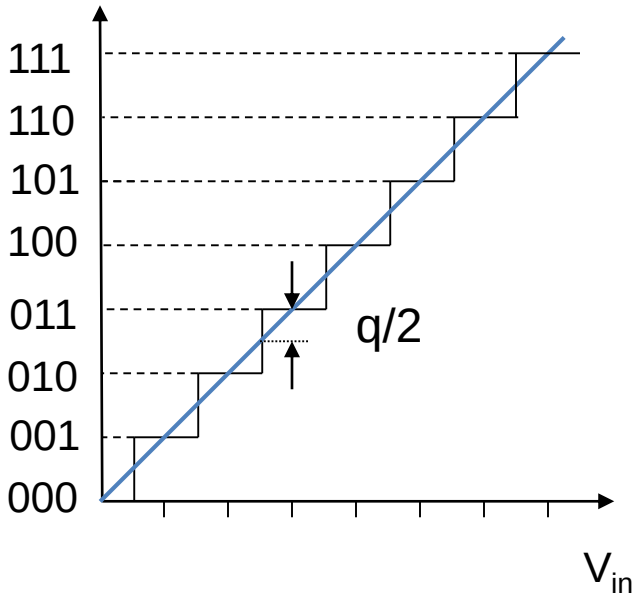
Aliasing





- If there is frequency component in the input signal above the Nyquist frequency at ω_M it will fold back into the baseband at $\omega s - \omega_M$ - this is called aliasing
- To prevent aliasing a A/D converter is usually preceded by an anti-aliasing filter, which is a low pass filter with a cut-off frequency of $\omega_s/2$

Digitising



- The sampling did not result in any information loss (in an ideal world), but the digitising will since only a limited number of bits is used to represent the analogue amplitude signal
- This error manifests itself as noise and can be treated as white noise in many cases
- The maximum quantisation error is $\pm q/2$

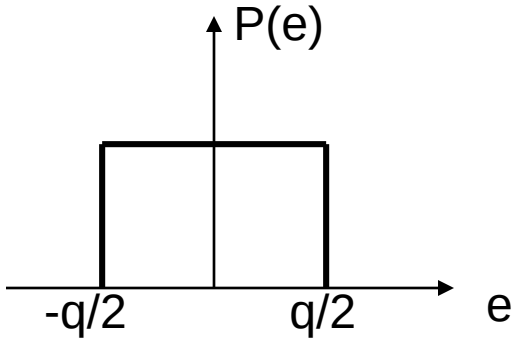
Terminology

- The number of quantisation levels for a N bit converter is 2^N
- The resolution is given by $V_{FS}/(2^N-1)$; (V_{FS}: full scale voltage). This is equivalent to the smallest increment level (or step size) q.
- MSB: Most significant bit: weighting of 2^{-1} V_{FS}
- LSB: Least significant bit: weighting of 2^{-N} V_{FS}
- Maximum output = $(1-2^{-N})$ V_{FS}
- Oversampling ratio: $OSR=f_s/2f_m$
- Monotonicity: a monotonic converter is one in which the output never decreases as the input increases. For A/D converters this equivalent to saying that it does not have any *missing codes.*

Example

- Example: An analogue signal in the range 0 to +10V is to be converted to an 8-bit digital signal. What is the resolution: What is the digital representation of an input signal of 6V and of 6.2V? What is the error made for the quantisation of 6.2V in absolute terms and as a percent of the input? As a percent of full scale? What is the max. quantisation error?

Quantisation Noise



- Assume the quantisation noise is uniformly distributed, the mean square value of the error can be calculated:

$$e_{qNS}^2 = \frac{1}{q}\int_{-q/2}^{q/2} e^2 de = \frac{q^2}{12} \qquad e_{RMS} = \frac{q}{\sqrt{12}}$$

- For a high number of bits the error is uncorrelated to the input signal (N>5). In the frequency domain the error appears as white over the Nyquist range.
- This noise limits the S/N ratio of the digital system analogous to thermal noise in an analogue system.

Signal to Quantisation Noise Ratio

- The peak value of a full scale sine wave (that is one whose peak to peak amplitude spans the whole range of the ADC) is given by: $2^N q/2$.
- The RMS of the sinewave is hence: $V_{RMS}=2^{N-1}q/\sqrt{2}$
- The signal to quantisation noise ratio (SQNR) is given by:

$$SQNR = \frac{2^{N-1}q/\sqrt{2}}{q/\sqrt{12}} = \sqrt{1.5}\cdot 2^N$$

- For a high number of bits the error is uncorrelated to the input signal (N>5). In the frequency domain the error appears as white over the Nyquist range.
- This noise limits the S/N ratio of the digital system analogous to thermal noise in an analogue system.

Oversampling

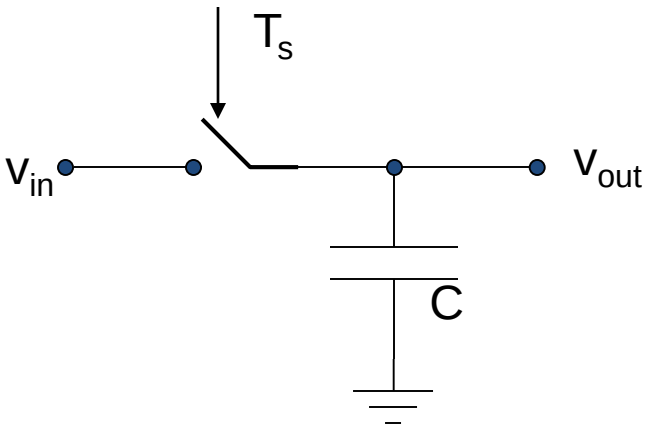
- The previous calculation assume that the input signal is sampled at the Nyquist rate
- The power spectral density of white quantisation noise is given by: $E^2(f)=e^2_{RMS} \bullet 2/f_s$
- The noise power is given by: $n_0^2 = \int_0^{f_m} E^2(f)df = e_{RMS}^2(2\frac{f_m}{f_s}) = \frac{e_{RMS}^2}{OSR}$

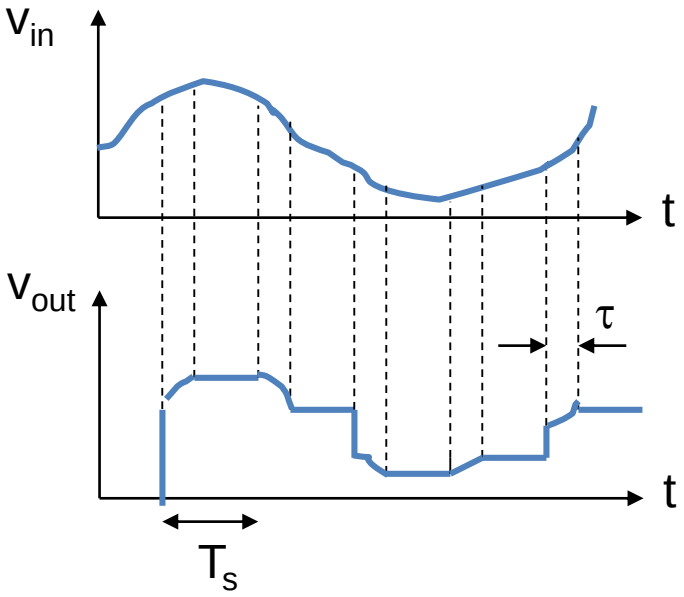
- SQNR is then:

$$SQNR = \frac{2^{N-1} q/\sqrt{2}}{q/\sqrt{12 \cdot OSR}} = \sqrt{1.5 \cdot OSR} \cdot 2^N$$

- or in dB: SQNR = (6.02 N + 1.76 + 20log($\sqrt{}$OSR))dB
- Thus doubling of the oversampling ratio only increases the SQNR by appr. 3dB or half a bit.

Sample & Hold





- usually: $\tau << T_s$ (for mathematical analysis $\tau = 0$)
- v_{out} often buffered before subjected to the A/D converter

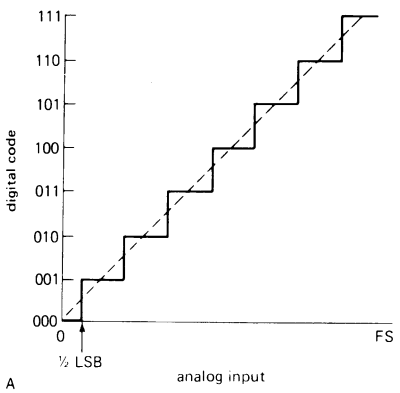
A/D Converter Types

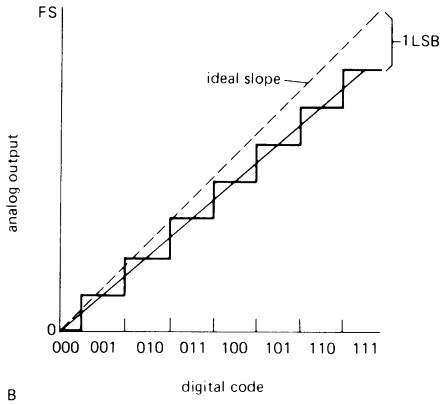
Specifications:

- Number of bits (typical 8 – 20)
- Sampling rate (typical 50Hz to 100MHz)
- Relative Accuracy: Deviation of the output from a straight line drawn through zero and full scale
  - Integral non-linearity or linearity
  - Differential linearity: Measure of step size variation. Ideally each step is 1 bit but in practice step sizes can vary significantly
  - Usually converters are designed so that they have a linearity better than ½ bit (if this were not the case then the LSB is meaningless)
- Monotonicity: No missing codes (i.e. 1001 -> 1011)
- Signal to Noise Ratio (same as Dynamic Range)

Errors

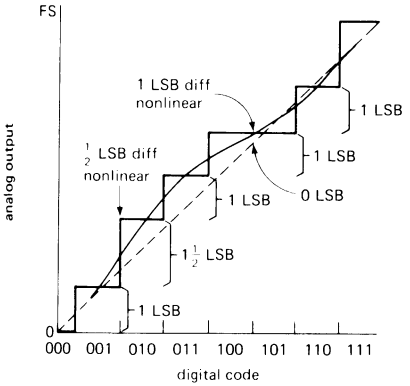
Offset error

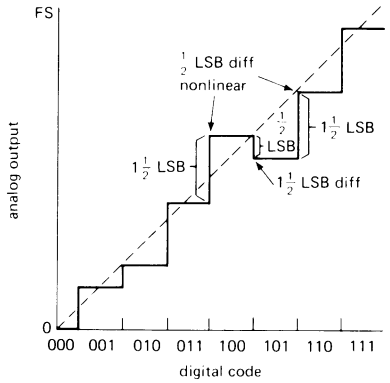




Linearity error
1LSB scale error

Non-linearity
1LSB differential
non-linearity

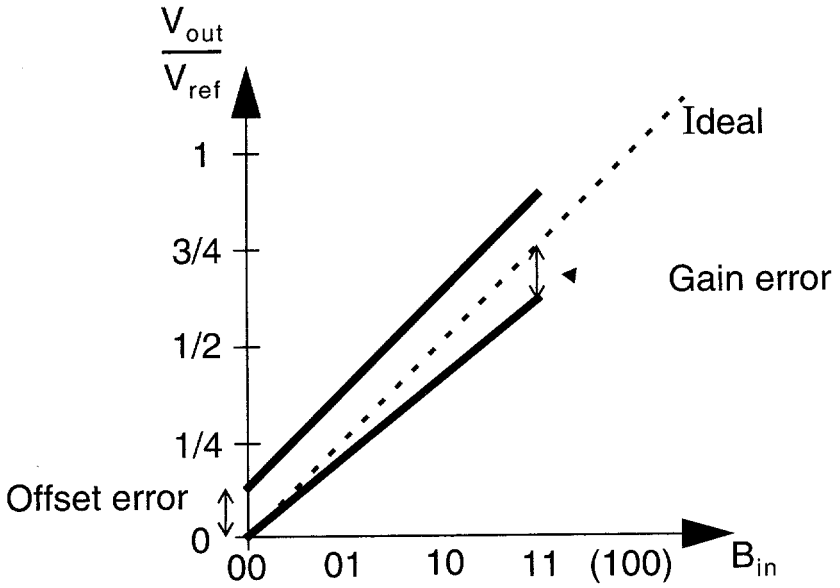




Non-monoticity
(implies a differential non-linearity of more than 1LSB)

- Errors originate from component tolerances, temp. sensitivity, noise in the electric circuit, etc

Offset and Gain Error



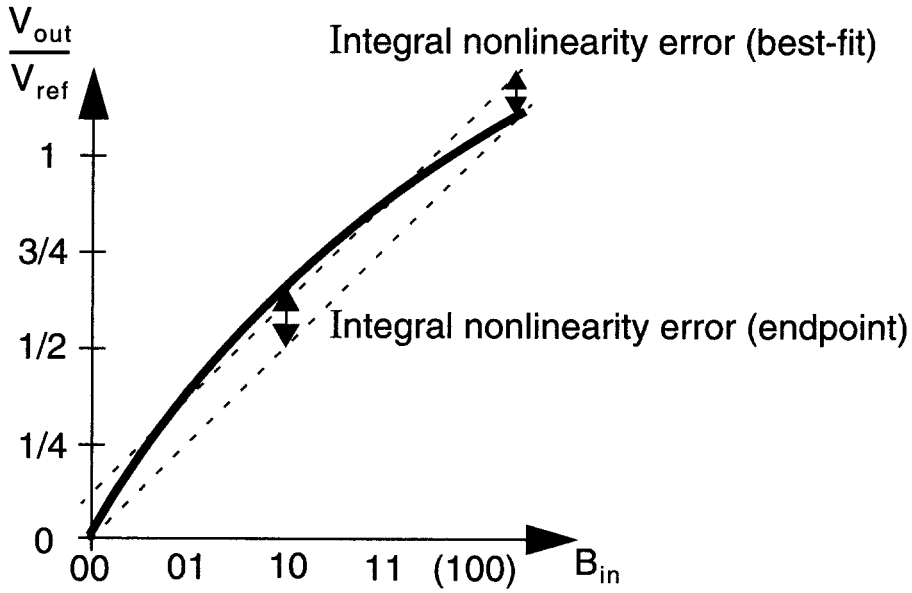
- Offset error is defined as the deviation of the voltage produced for the 000…01 code from ½ V_{LSB}.

$$E_{OFF} = \frac{V_{0...01}}{V_{LSB}} - \frac{1}{2}V_{LSB}$$

- Gain error is defined as the difference at the full scale value between the ideal and actual curve when the offset error has been removed. It is given in units of LSB.

$$E_{gain} = \left(\frac{V_{1...11}}{V_{LSB}} - \frac{V_{0...01}}{V_{LSB}}\right) - \left(2^N - 2\right)$$

Integral/Differential Nonlinearity Error



- For an ideal A/D converter each transition value is precisely 1 LSB apart.
- Differential nonlinearity (DNL) is defined as the variation in step sizes away from 1 LSB (after gain and offset errors have been removed).

- After both the offset and gain errors have been removed, the *integral nonlinearity* (INL) is defined to be the deviation from the straight line.
- Two straight lines can be used: endpoints of the converter's transfer characteristics or a best fit.
- In the literature INL is either used to describe the maximum deviation from the straight line or the deviation from the straight line for each digital word.

Example

An analogue signal 0..10V is to be digitised with an quantisation error less than 1% of full scale. How many bits are required?

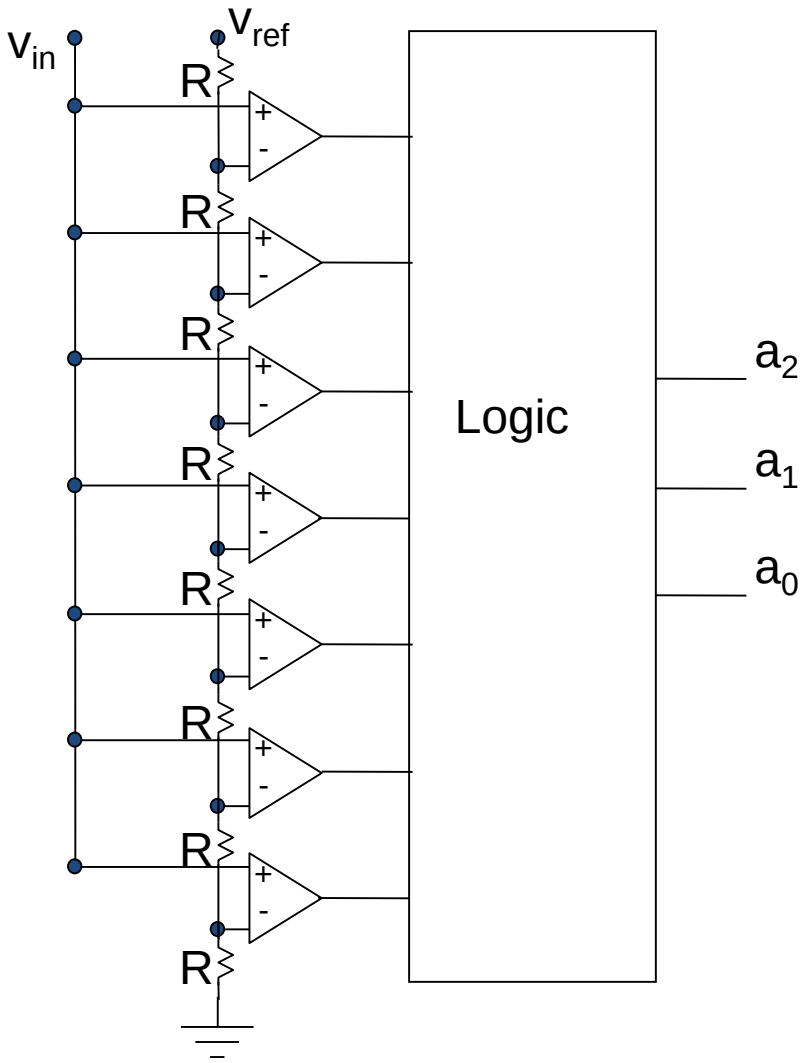
How many bits are required if the range is extended to $\pm$10V (for the same resolution)?

What is the resolution and quantisation error ?

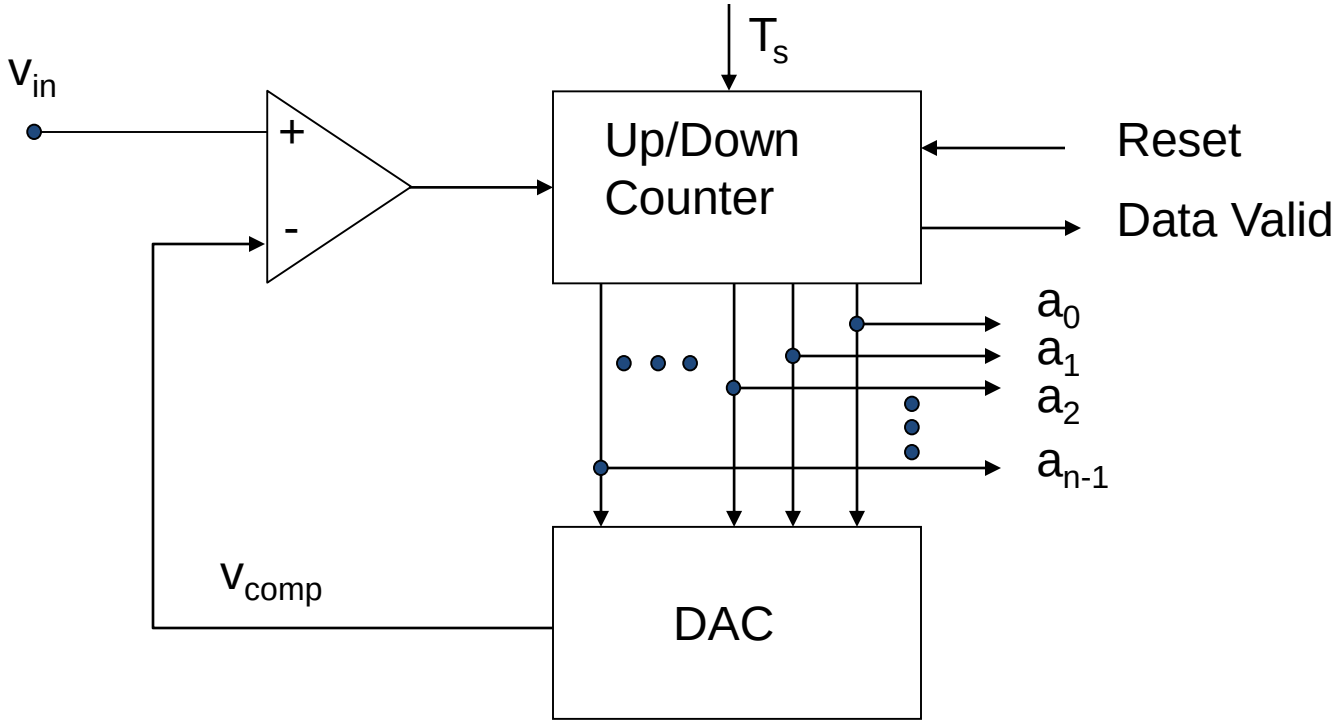
Flash Converter

Example:
3 bit flash converter

- requires 2^N-1 comparators and 2^N resistors
- fastest converter; conversion can be performed in one clock cycle
- high circuit complexity
- accuracy depends on resistor matching and comparator performance (practical up to 8Bits)

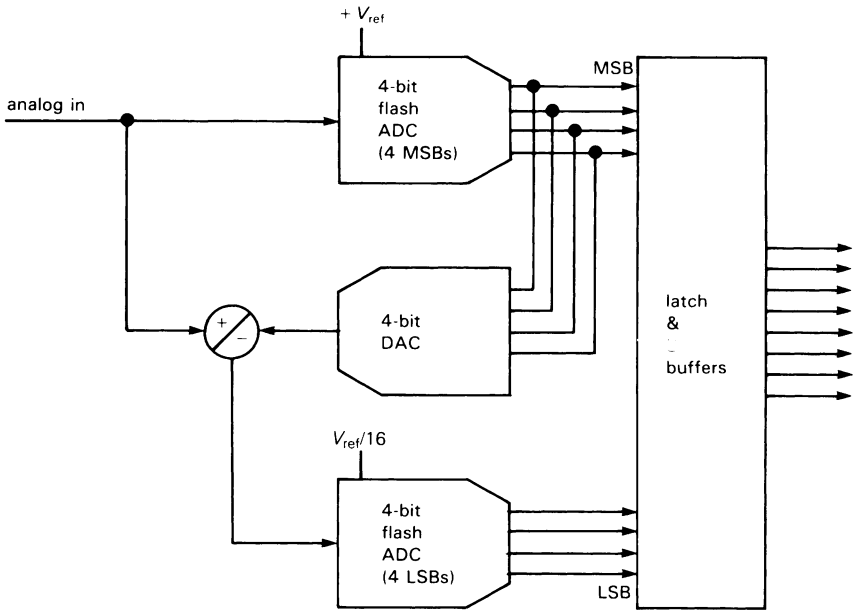


Counting (Feedback) Converter



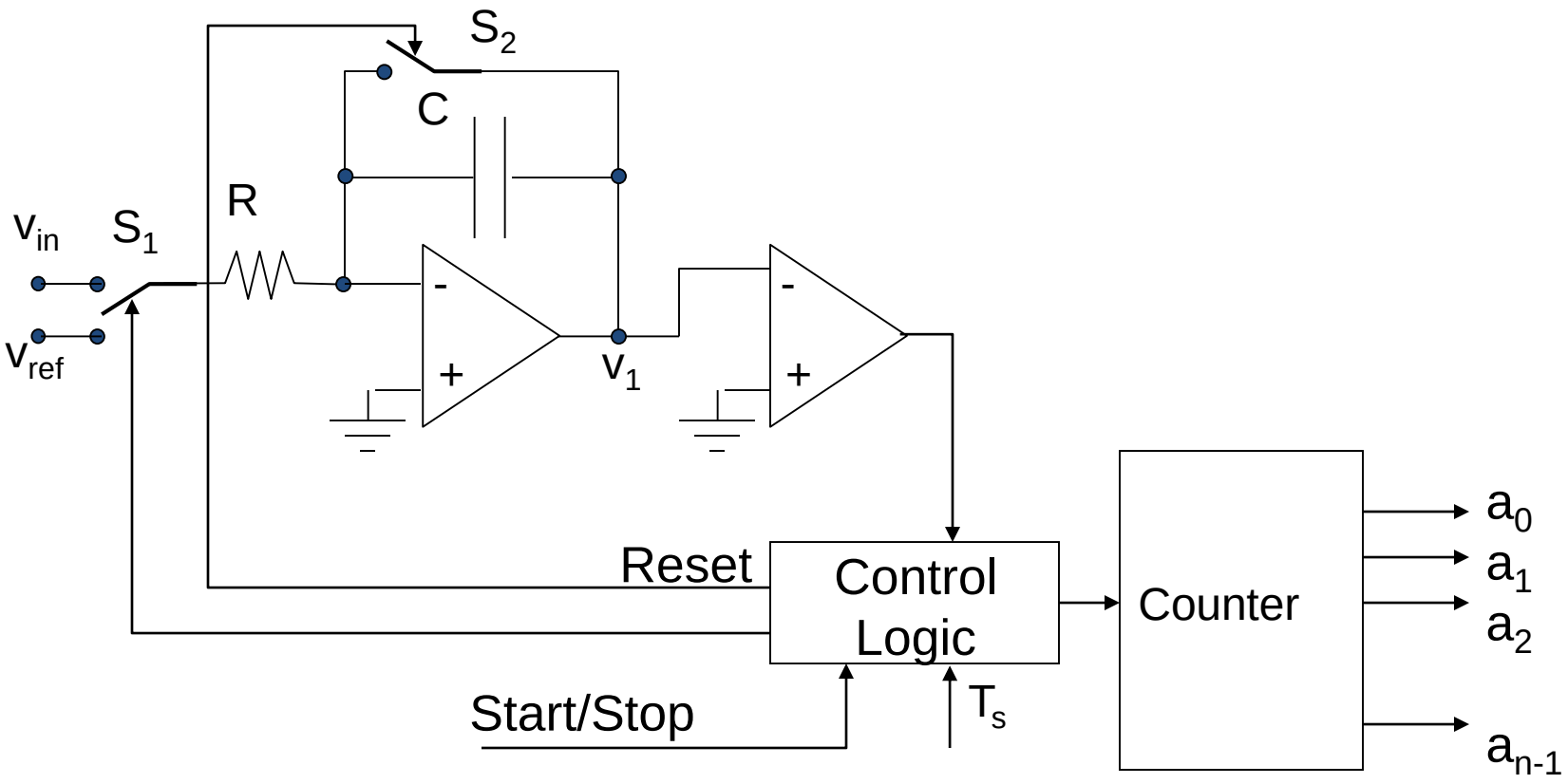
- easy to implement
- conversion speed depends on difference to previous sample ⇒ slow for fast varying signals, fast for slowly varying signals (⇒ oversample)
- “tracking or counting A/D converter”

Half-Flash Converter



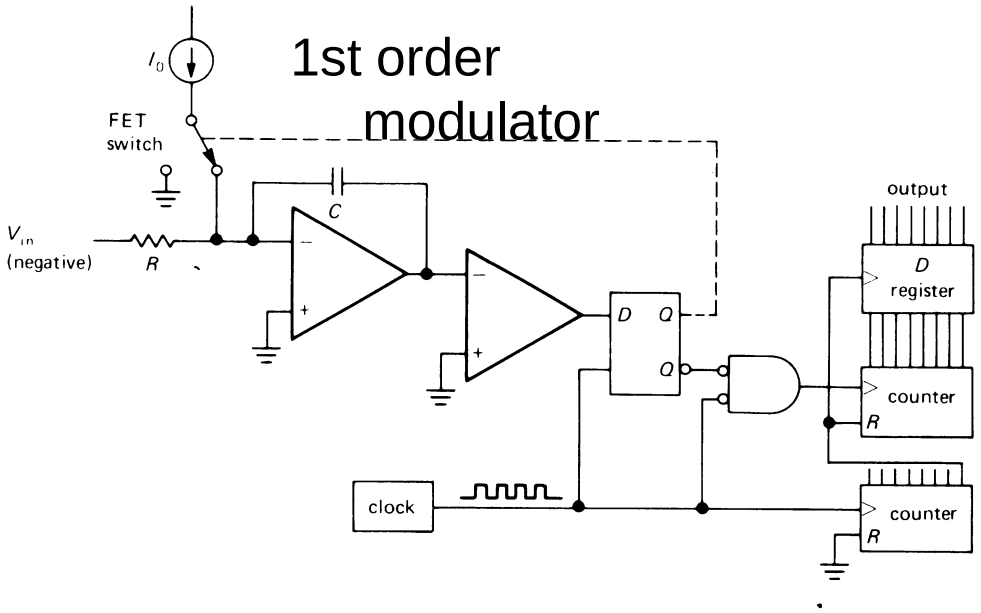
- hybrid solution: good compromise between speed and circuit complexity
- use separate flash converter for higher bits and lower bits
- e.g. for 8 bits: $2 \cdot 2^4$ comparators needed instead of $2^8 = 256$.

Dual Slope ADC

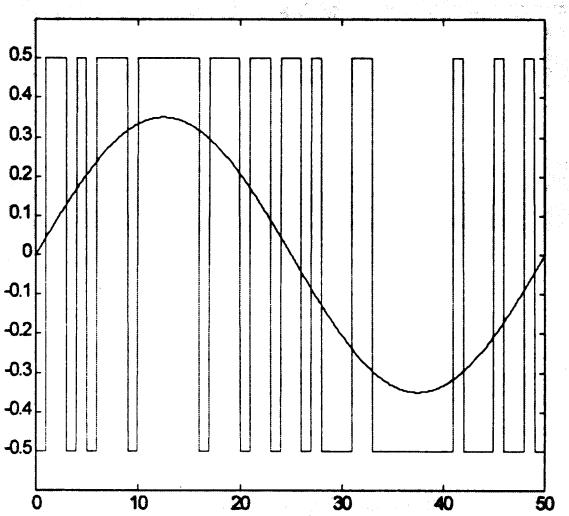


- high resolution (up to 14 bits) ADC's
- independent of exact values of R and C
- implementation in CMOS
- relatively slow

Sigma-Delta Modulators (ΣΔM) A/D Converters

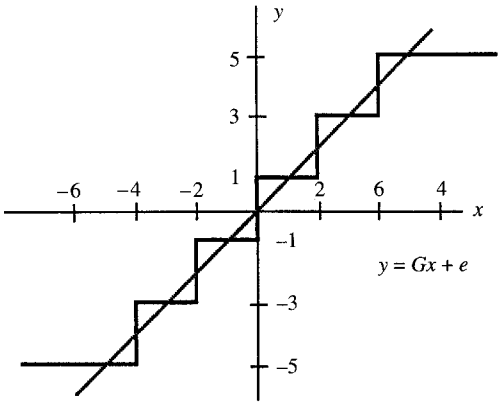


Typical waveform:
pulse density modulation

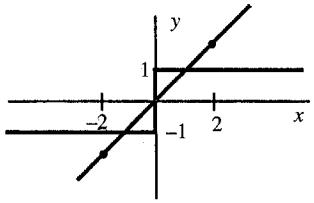


- extremely high resolution (up to 20 bits) ADC's
- only one reference signal is required
- oversampling is required; $f_s >> f_{nyquist}$
- difficult to analyse $\Rightarrow$ use simulation
- in many commercial devices (CD players, mobile phones, etc)
- suitable for VSLI implementation

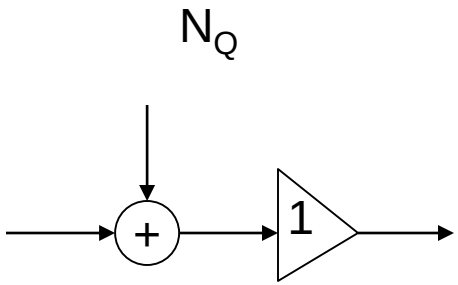
One Bit Quantiser



Multibit quantiser

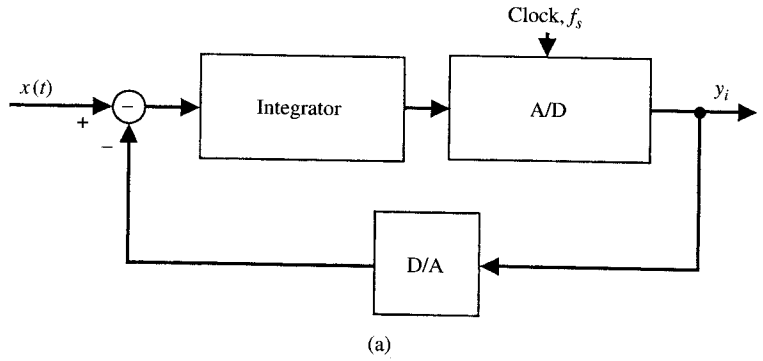


1bit quantiser

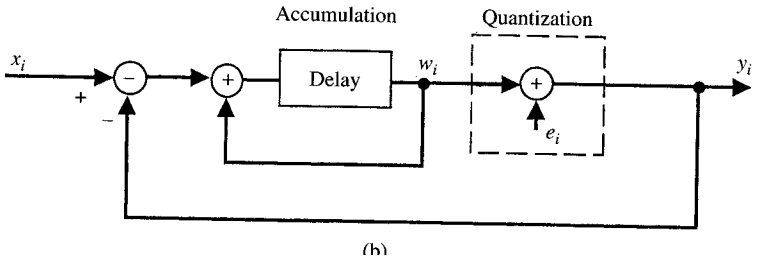


- A one bit quantiser is always linear since the gain is arbitrary.
- The quantiser can be modelled by a (quantisation) noise source and a gain of 1

First Order ΣΔM



(a)



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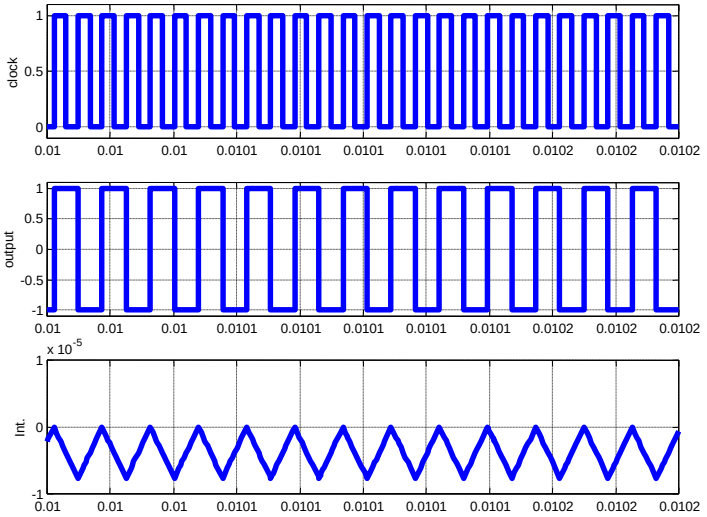
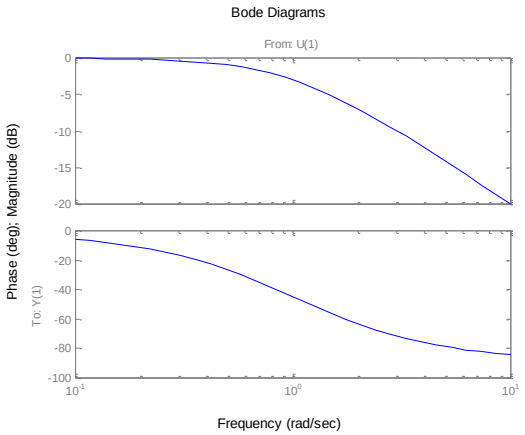


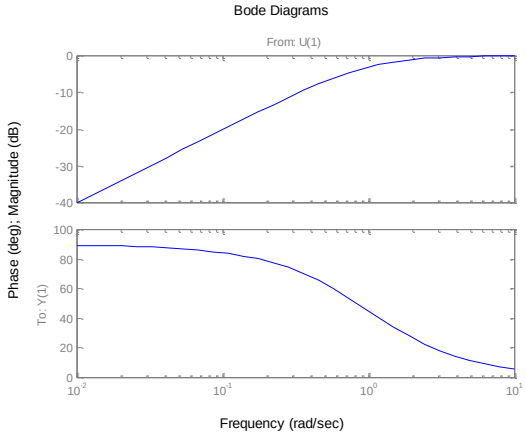
- First order modulators can be easily simulated and analysed
- However, they only provide first order noise shaping
- For zero input we get alternating ‘1’s and ‘0’s at the output with a frequency of $f_s/2$. The average of this bitstream is 0.
- If the input is positive, there will be more ‘1’s than zero, the average over a number of clock pulses is then a measure of the input.

1st Order ΣΔM – Noiseshaping

Signal Transfer Function

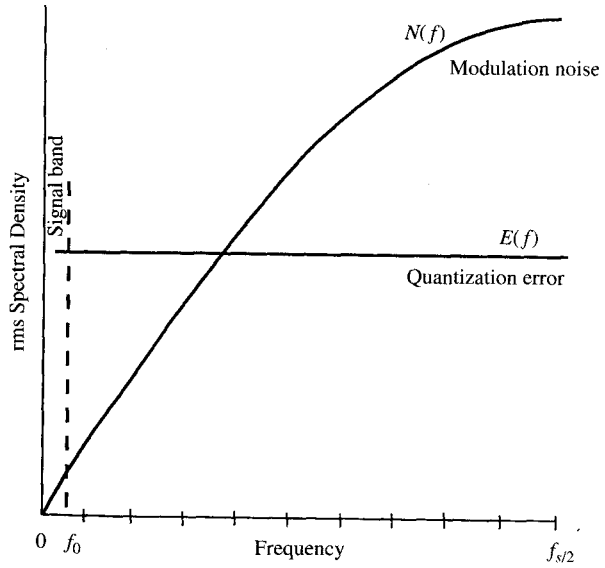


Noise Transfer Function



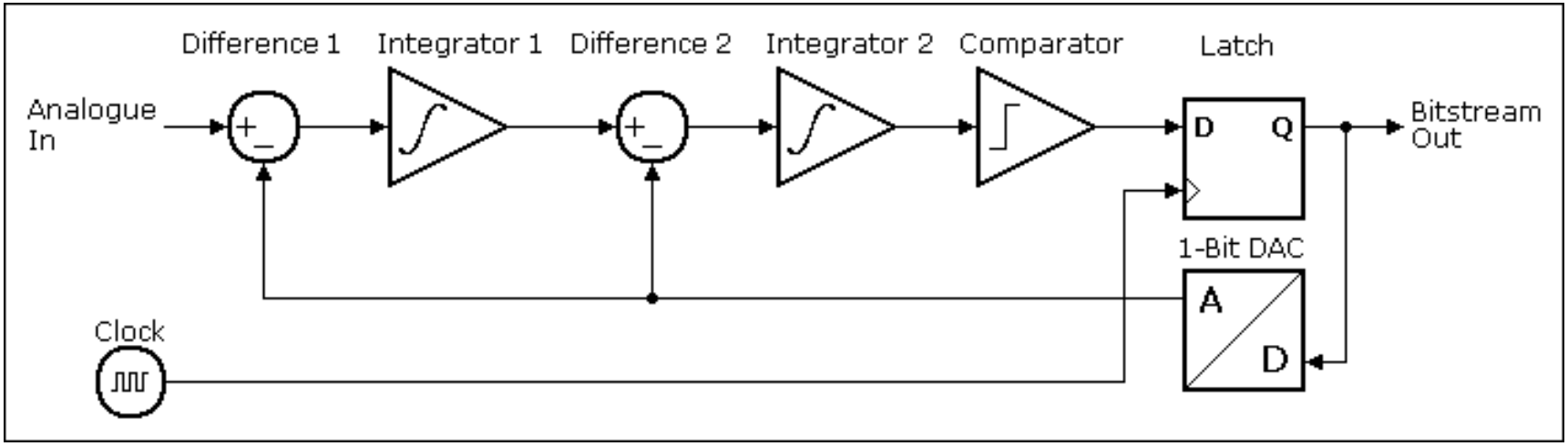
- Signal Transfer Function: STF=1/(s+1) ⇒ Low pass filtered
- Noise Transfer Function: NTF=s/(s+1) ⇒ High pass filtered, thus the noise is attenuated at lower frequencies in the signal band (Noise shaping).

1st Order ΣΔM – Noiseshaping



- Noise spectral density is shaped as shown above.
- Clearly feedback around the quantiser reduces the noise spectral density at low frequency but increases at high frequencies.
- Above example is plotted for OSR = 16.

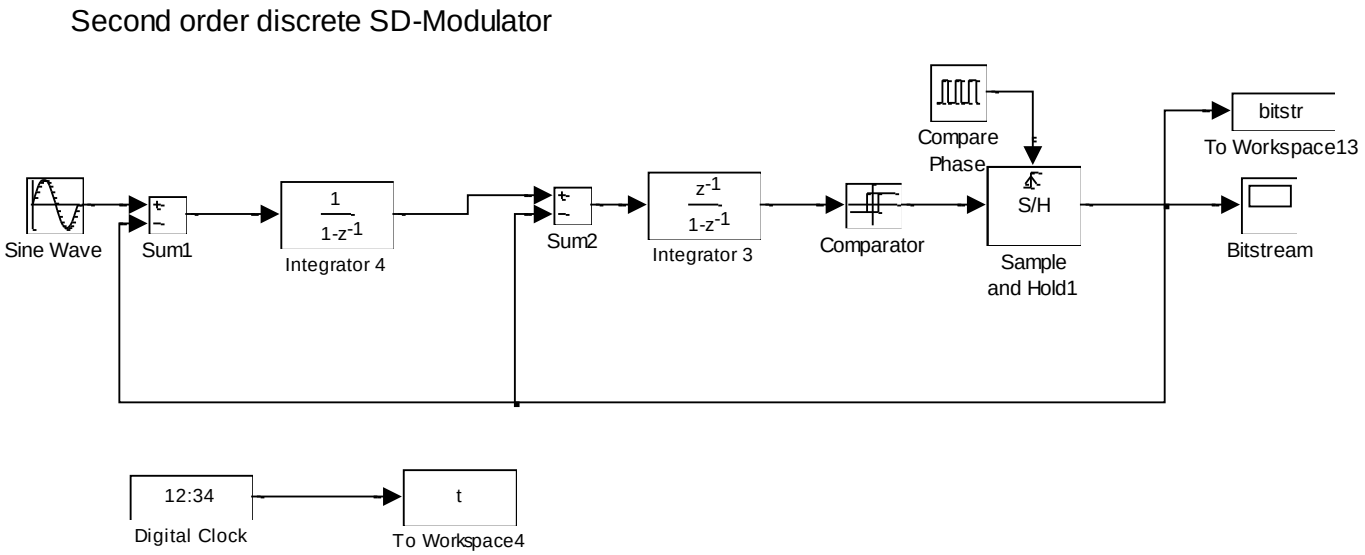
Second Order ΣΔM



- If better noise shaping is required a second order modulator can be used.
- A second order modulator can be analysed in exactly the same way as a first order modulator.
- NTF: $(1-z^{-1})^2$; STF: z-1
- Noise Power Spectral Density: $N_q^2(f)=32e^2_{RMS}T_s\sin^4(\omega T_s/2)$
- RMS Noise in the signal band:

$$n_0 = \int_0^{f_B} \left|N_q(f)\right|^2 df = e_{RMS}\frac{\pi^2}{\sqrt{5}}OSR^{-5/2}$$

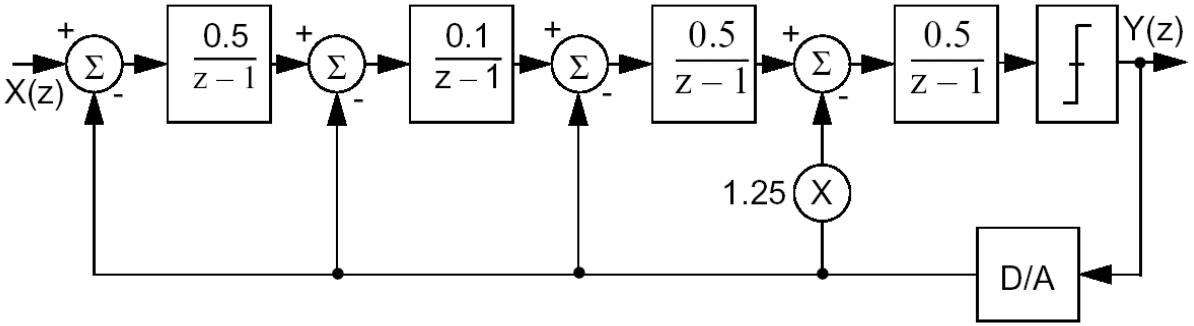
Second Order ΣΔM

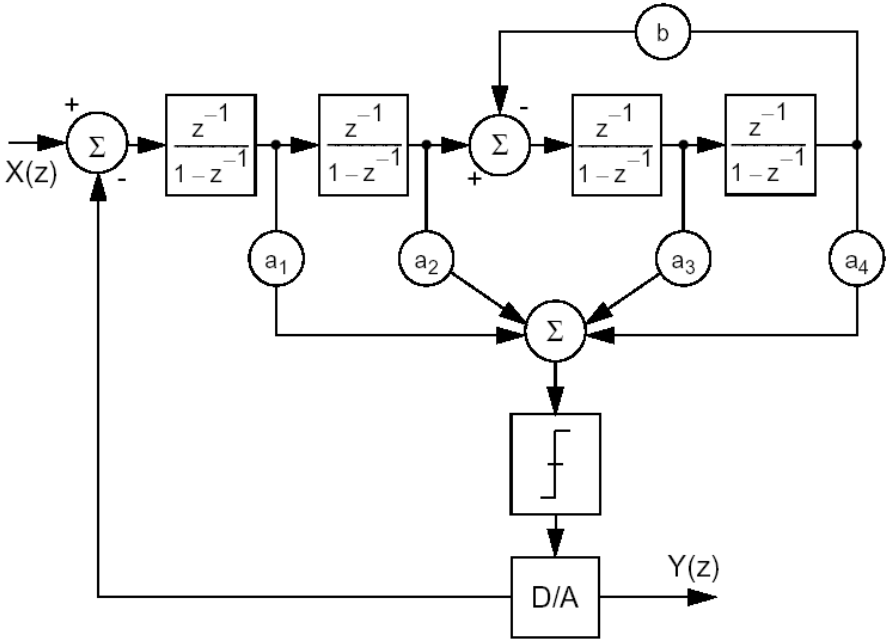


- Simulink simulation model
- Discrete second order model

Higher Order ΣΔM

4th order ΣΔM;
basic architecture





4th order ΣΔM
Interpolative architecture

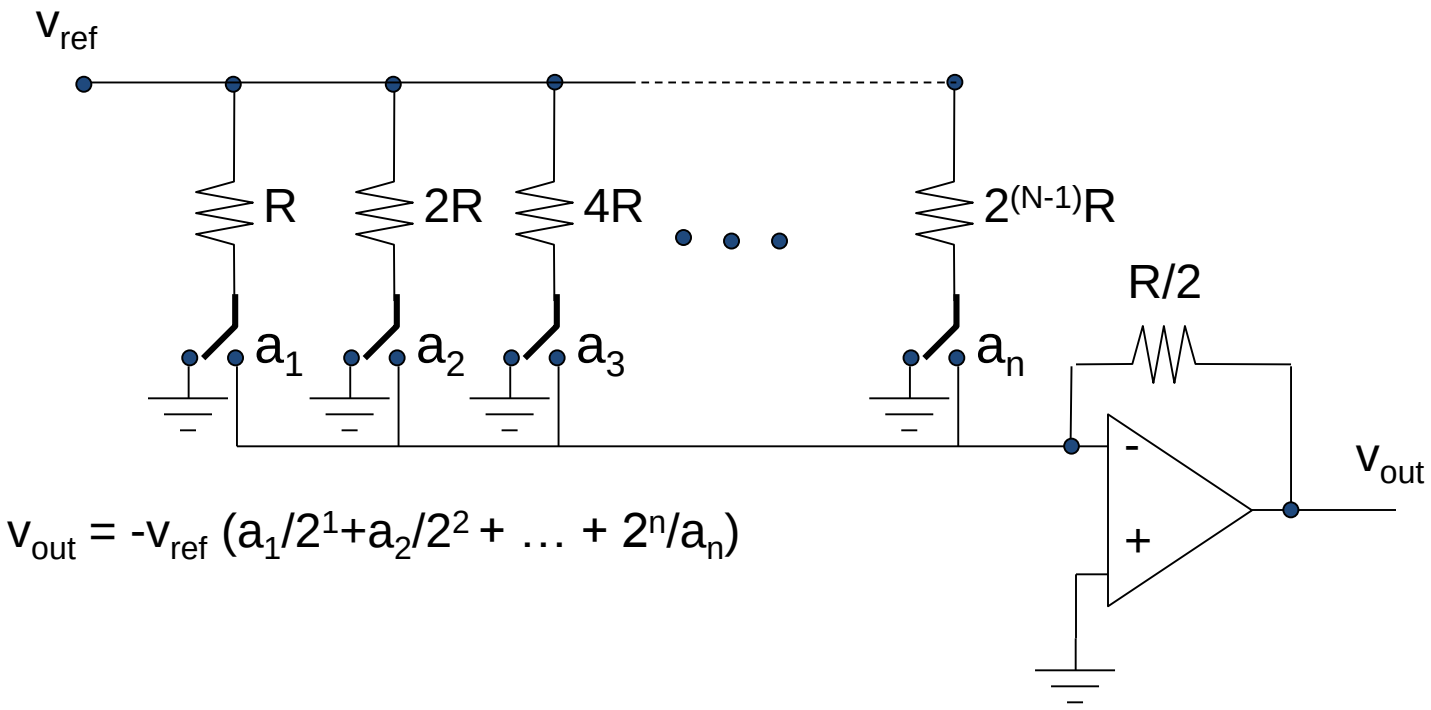
Example

- A second order modulator with a one bit quantiser (quantisation levels +1 and –1) is clocked at 1MHz. It is used to convert audio signals with a bandwidth of 40kHz.
- Calculate:
  - the oversampling ratio
  - The signal to quantisation noise ratio (SQNR) assuming a full scale sinewave at the input.
  - How much does the SQNR improve if the sampling frequency is increased to 2MHz?

D/A Background

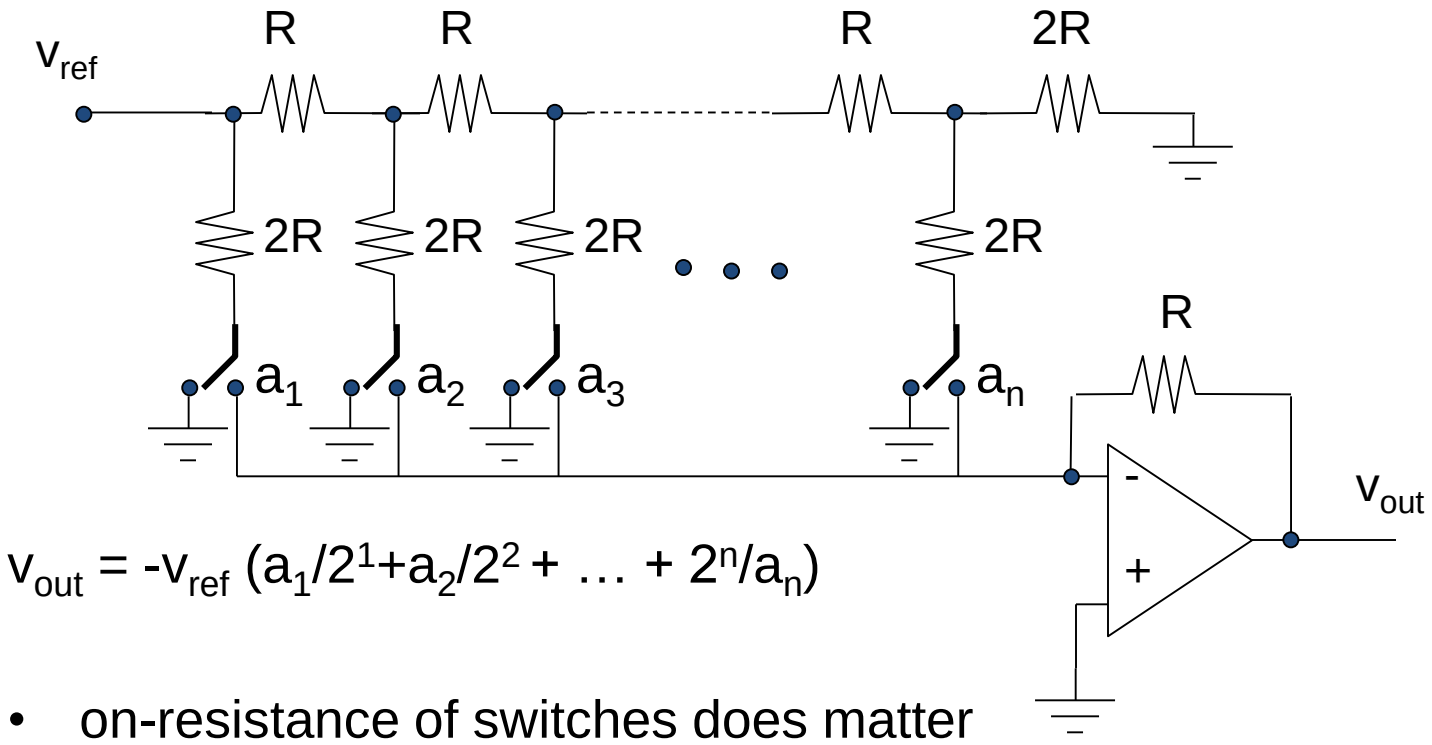
- Convert a digital number into an analogue voltage
- Analogue signals are typically required for actuating a physical system (e.g. loudspeaker, moving coil meter, etc)
- Weight of each increases by factor of 2:
- $V_{out} = (a_1/2^1 + a_2/2^2 + \ldots + a_n/2^n)\, V_{ref}$
- a_1: MSB; a_n: LSB
- Many D/A conversion methods exist, trade-off between bandwidth, accuracy, circuit complexity.

Binary Weighted Resistors



- For n large: resistor value spread is huge
- on-resistance of switches does matter

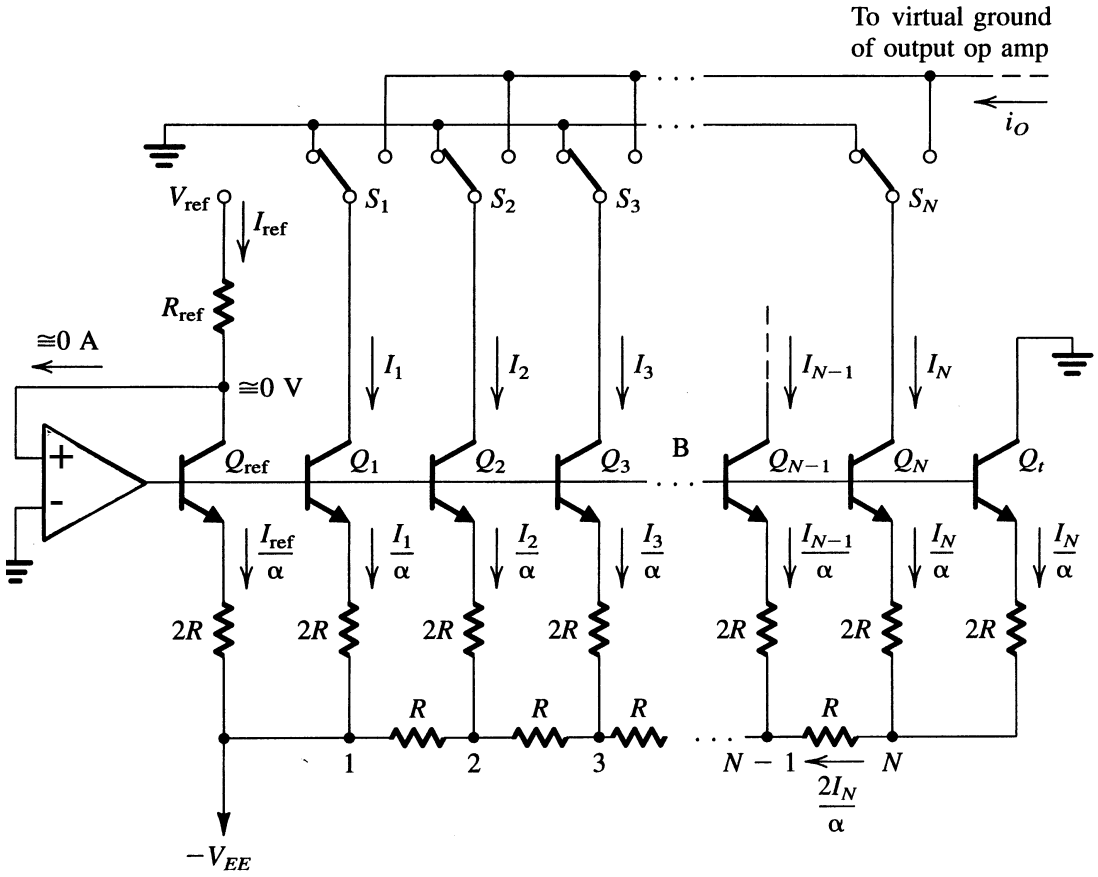
R-2R Ladder Network



$$v_{out} = -v_{ref} (a_1/2^1 + a_2/2^2 + \ldots + 2^n/a_n)$$

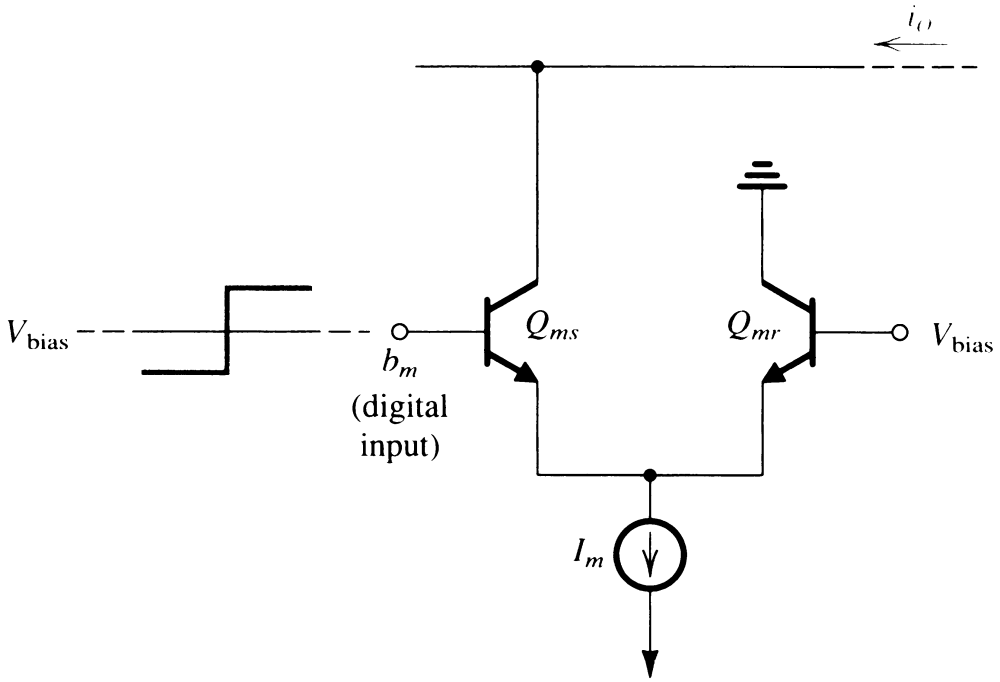
- on-resistance of switches does matter
- resistor value spread is much smaller
- accuracy depends on absolute resistance values

Practical R-2R Ladder Network



- use BJT to produce binary weighted currents

Current Switch



- use MOST to reduce base current error